the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform,

a low pass filter coupled to said integrator charge storage means for deriving a mean d.c. voltage level of said time varying voltage waveform, and

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

2. (Amended) An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and said low pass filter defines a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage level substantially constant.

Please cancel claim 5.

~~6.~~ (Amended) An anti-jitter circuit as claimed in claim 1 wherein the low pass filter comprises the combination of a resistor and a capacitor.

~~12.~~ (Twice Amended) An anti-jitter circuit as claimed in claim ~~8~~ 6 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. voltage level.

~~13.~~ (Twice Amended) An anti-jitter circuit as claimed in claim 1 comprising a first ~~said~~ charging means and a second ~~said~~ charging means for deriving charge packets

respectively from the rising and falling edges of the input pulse train, said first and second charging means being effective as a frequency doubling means.

28 ~~27~~. (Amended) An anti-jitter circuit as claimed in claim 1 wherein said charging means is a charge pump.

14 ~~20~~. (Amended) An anti-jitter circuit as claimed in claim ~~29~~ 13 wherein said low pass filter comprises the combination of a resistor and a capacitor.

IN THE ABSTRACT:

Please add the following Abstract (also attached on a separate sheet):

An anti-jitter circuit has an integrator/storage capacitor. A charge pump derives from an input pulse train at least one charge packet during each cycle of the input pulse train and supplies the charge packets to the storage capacitor. A controlled current sink operating in conjunction with a high impedance low pass filter continuously discharges the storage capacitor to create a sawtooth voltage waveform having a mean d.c. voltage level. A differential comparator compares the sawtooth voltage waveform with the mean d.c. voltage level and the comparator output is used to trigger a monostable circuit to generate an output pulse train having reduced time jitter